Electronic Version
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Claims

[c1] 1. A pixel structure, comprising:
a scan line, disposed overa substrate;
a data line, disposed over the substrate;
an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;
a plurality of transparent capacitance electrodes, disposed over the substrate; and
a pixel electrode, disposed over the transparent capacitance electrodes and electrically connected to the active component, wherein the pixel electrode and the transparent capacitance electrodes constitute a multilayer pixel storage capacitor.

[c2] 2. The pixel structure of claim 1, wherein a portion of the transparent capacitance electrode is electrically connected to the active component.

[c3] 3. The pixel structure of claim 1, wherein a portion of the transparent capacitance electrode is electrically connected to the pixel electrode, and electrically connected to the active component via the pixel electrode.

[c4] 4. The pixel structure of claim 1, wherein the active component comprises a low temperature polysilicon (LTPS) thin film transistor (TFT).

[c5] 5. The pixel structure of claim 4, further comprising:
a source/drain conductive layer, wherein the active component is electrically connected to the data line and the pixel electrode via the source/drain conductive layer.

[c6] 6. The pixel structure of claim 4, further comprising:
a conductive layer, wherein the active component is electrically connected to the data line via the conductive layer, and the pixel electrode is electrically connected to the active component.

[c7] 7. The pixel structure of claim 1, wherein the active component comprises an amorphous silicon (a-Si) thin film transistor (TFT).

[c8] 8. The pixel structure of claim 7, wherein the active component comprises:
a gate, electrically connected to the scan line;
a channel, disposed over the gate; and
a source/drain, disposed over the channel and electrically connected to the data line and the pixel electrode.

[c9] 9. The pixel structure of claim 1, wherein a material of

the pixel electrode and the transparent capacitance electrode comprise an indium tin oxide (ITO) oran indium zinc oxide (IZO).

[c10] 10. A manufacturing method, for a pixel structure, comprising:
sequentially forming an active component, a scan line and a data line over a substrate, wherein the active component is electrically connected to the scan line and the data line;
forming a plurality of transparent capacitance electrodesover the substrate; and
forming a pixel electrode over the transparent capacitance electrodes, wherein the pixel electrode is electrically connected to the active component, wherein the pixel electrode and the transparent capacitance electrodes constitute a multilayer pixel storage capacitor.

[c11] 11. The manufacturing method of claim 10, wherein the active component comprises a low temperature polysilicon (LTPS) thin film transistor (TFT).

[c12] 12. The manufacturing method of claim 11, wherein a source/drain conductive layer over the active component duringthe step of forming the data line, wherein the active component is electrically connected to the data line and the pixel electrode via the source/drain conductive

layer.

[c13] 13. The manufacturing method of claim 11, further comprises a step of forming a conductive layer over the active component after the step of forming the data line, wherein the active component is electrically connected to the data line via the conductive layer, and the pixel electrode is electrically connected to the active component.

[c14] 14. The manufacturing method of claim 13, wherein the conductive layer and the pixel electrode is formed by patterning a same material layer.

[c15] 15. The manufacturing method of claim 11, wherein the step of forming the active component comprises:
forming a polysilicon layer over the substrate;
forming an inter-gate dielectric layer over the substrate covering the polysilicon layer;
forming a gate over the inter-gate dielectric layer and the polysilicon layer; and
forming a doped source/drain region in the polysilicon layer on both sides of the gate.

[c16] 16. The manufacturing method of claim 15, wherein the step of forming the doped source/drain region comprises:
performing anion implantation process using the gate as

a mask to form the doped source/drain region on both sides of the polysilicon layer.

[c17] 17. The manufacturing method of claim 10, wherein the active component comprisesan amorphous silicon (a-Si) thin film transistor (TFT).

[c18] 18. The manufacturing method of claim 17, wherein the step of forming the active component comprises:
forming a gate over the substrate, wherein the gate is electrically connected to the scan line;
forming an inter-gate dielectric layer over the substrate covering the gate;
forming a channel over the inter-gate dielectric layer, wherein the channel is disposed over the gate; and
forming a source/drain over the channel.

[c19] 19. The manufacturing method of claim 10, wherein a material of the pixel electrode and the transparent capacitance electrodes comprise an indium tin oxide (ITO) or an indium zinc oxide (IZO).